400G QSFP-DD SR8 Transceiver

OTQDD-40X85-SR8

Features

- 26.5625 GBd PAM 4×8 channel 400G-SR8 Optical interface
- 26.5625 GBd PAM 4×8 channel 400G AUI-8 C2M Electrical interface
- Up to 70m transmission distance on OM3 MMF
- 850nm VCSEL and PIN receiver
- QSFP-DD MSA package with MPO-16
- Very low EMI and excellent ESD protection
- +3.3V power supply
- Power consumption less than 11W
- Operating case temperature: 0~+70°C
- IIC rate up to 400KHz

Applications

- 400GEthernet
- Datacenter switch

Compliance

- QSFP-DD MSA
- IEEE 802.3cm
- IEEE 802.3cd
- CMIS Rev4.0
- RoHS compliance
- GR-468-CORE

Description

The HG Genuine OTQDD-40X85-SR8 Transceiver is a high performance, cost effective module for serial optical data communication applications to 400Gbps, The OTQDD-40X85-SR8 is designed to Datacenter, accept 400G Ethernet protocol traffic for 70m links.

The module mainly consists of two parts: the transmitter part and the receiver part. The transmitter part consists of 8chs 850nm VCSEL array and driver. The receiver part consists of 8chs trans-impedance amplifier (TIA) and PIN photodiode array.

The high-speed electrical interface is based on low-voltage logic, with nominal 100ohm differential impedance, AC coupled inter of module.

Users can access to a series of registers to monitor and configurate data through two wire serial interface.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Storage Temperature	T_S	-40		85	℃	
Supply Voltage	V_{CC3}	3.1		3.6	V	
Relative Humidity(Non-Condensing)	RH	5		85	%	Note1
Rx Input Power	P_{max}			5	dBm	

Notes:

[1] Non-condensing

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Case Temperature	T_C	0		70	℃	
Power Supply	V_{CC3}	3.135	3.3	3.465	V	
	I_{CC3}			3350	mA	
Power Dissipation	P_D			11	W	
Data Rate per channel (PAM4)			26.5625		GBd	
Signaling Speed Accuracy		-100		100	ppm	
Transmission Distance(OM3)				70	m	
Transmission Distance(OM4)				100	m	

Optical，Electrical Characteristic

Table3-Transmitter Operating Characteristic-Optical，Electrical

Parameter	Symbol	Min	Typ	Max	Unit	Note
Center Wavelength	λ_C		850		nm	
Spectral Width(RMS)	RMS			0.6	nm	Note1
Laser Off Power	P_{off}			-30	dBm	
Average Optical Power	P_{avg}	-6.5		4	dBm	
Extinction Ratio	ER	3			dB	
Transmitter and dispersion eye closure	TDECQ			4.5	dB	
Outer Optical Modulation Amplitude	OMA_{outer}	-4.5		3		Note2
Encircled flux, each lane	EF		≥ 86% @ 19 μm, ≤ 30% @ 4.5 μm			Note3
Transition time, each lane (max)				34	ps	
Optical Return Loss Tolerance				12	dB	
Operating Data Rate, each lane			26.5625		GBd	

Notes:

[1] RMS spectral width is the standard deviation of the spectrum.

[2]Even if the TDECQ<1.4dB,the OMA(min) must exceed this value.

[3]If measured into type A1a.2, type A1a.3 or type A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.

Table4-Receiver Operating Characteristic-Optical，Electrical

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Data Rate,each lane			26.5625		GBd	
Modulation format			PAM4			
Center Wavelength	λ_r	840	850	860	nm	
Damage threshold		5			dBm	
Average receive power		-8.4		4	dBm	Note3
Receiver sensitivity (OMA_{outer})	RS	-	-	-	dBm	Note1、2
Receiver Reflectance				-12	dB	
Differential Data Output Voltage Peak to Peak Swing	V_{opp}			900	mV	
Differential output Impedance	Z_{os}	90	100	110	ohms	
Common Mode Voltage	V_{cm}	-0.35		2.85	V	
Common Mode Noise RMS				17.5	mV	
Differential output return loss	SDD22	Per OIF CEI-56G-VSR-PAM4 and 400GAUI-8 requirements			dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion	SDC22, SCD22					
Common Mode Return Loss	SCC22			-2	dB	

Notes:

[1]Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5dB.

[2]RS=max（-6.5，SECQ-7.9）(dB)

[3]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

RS: is the receiver sensitivity

SECQ: is the SECQ of the transmitter used to measure the receiver sensitivity

Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Table5- Digital Diagnostic Functions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3		3	℃	Over operating temperature
Tx power monitor absolute error	DMI_TX	-3		3	dB	
Rx power monitor absolute error	DMI_RX	-3		3	dB	
Supply voltage monitor absolute error	DMI_VCC	-3		3	%	Over operating voltage
Bias current monitor absolute error	DMI_Ibias	-10		10	%	

Notes:

The reported temperature is measured by the temperature of the shell near the DSP.

Table6-Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
MgmtInitDuration	Max MgmtInit Duration			2000	ms	Note1
ResetL Assert Time	t_reset_init	10			μs	Note2
IntL Assert Time	ton_IntL			200	ms	Note3
IntL De-assert Time	toff_IntL			500	μs	Note4
Rx LOS Assert Time	ton_los			100	ms	Note5
Rx LOS Assert Time (optional fast mode)	ton_losf			1	ms	Note6
Rx LOS De-assert Time (optional fast mode)	toff_losf			3	ms	Note7
Flag Assert Time	ton_flag			200	ms	Note8
Mask Assert Time	ton_mask			100	ms	Note9
Mask De-assert Time	toff_mask			100	ms	Note10

Notes:

[1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.

[2] Minimum pulse time on the ResetL signal to initiate a module reset.

[3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol.

[4] Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes de-assert times for Rx LOS, Tx Fault and other flag bits.

[5] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.

[6] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.

[7] Time from signal present to negation of Rx LOS status bit.

[8] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.

[9] Time from mask bit set (value=1b) until associated IntL assertion is inhibited.

[10] Time from mask bit cleared (value=0b) until associated IntL operation resumes.

Pin-out Definition

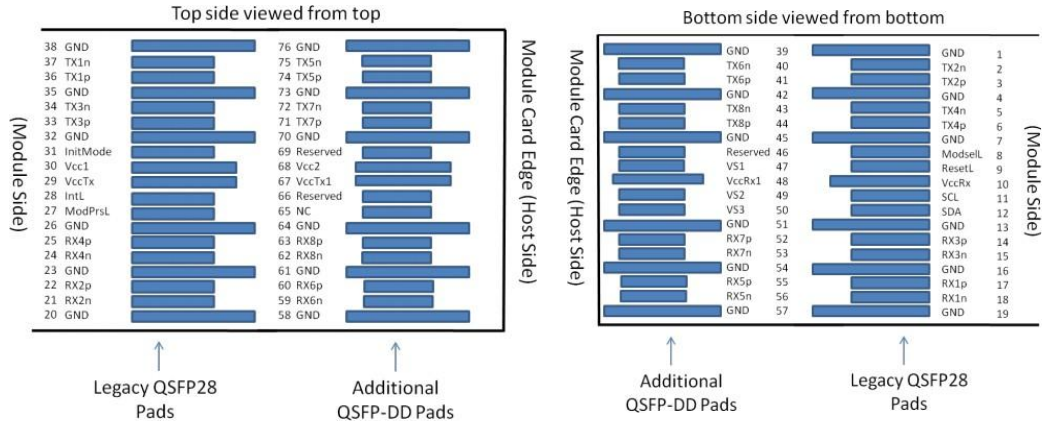

Figure1

Table7-Pin Function Definitions

Pad	Logic	Symbol	Name/Description	Plug Sequence[4]	Note
1		GND	Ground	1B	Note1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	Note1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	Note1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	3.3V Power Supply Receiver	2B	Note2
11	LVCMOS–I/O	SCL	2 wire serial interface clock	3B	
12	LVCMOS–I/O	SDA	2 wire serial interface data	3B	
13		GND	Ground	1B	Note1
14	CML-O	Rx3n	Transmitter Inverted Data Output	3B	
15	CML-O	Rx3p	Transmitter Non-Inverted Data Output	3B	
16		GND	Ground	1B	Note1
17	CML-O	Rx1n	Transmitter Inverted Data Output	3B	
18	CML-O	Rx1p	Transmitter Non-Inverted Data Output	3B	
19		GND	Ground	1B	Note1
20		GND	Ground	1B	Note1
21	CML-O	Rx2n	Transmitter Inverted Data Output	3B	
22	CML-O	Rx2p	Transmitter Non-Inverted Data Output	3B	
23		GND	Ground	1B	Note1
24	CML-O	Rx4n	Transmitter Inverted Data Output	3B	

25	CML-O	Rx4p	Transmitter Non-Inverted Data Output	3B	
26		GND	Ground	1B	Note1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccRx	3.3V Power Supply Transmitter	2B	Note2
30		Vccl	3.3V Power Supply	2B	Note2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	Note1
33	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
34	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
35		GND	Ground	1B	Note1
36	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
37	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
38		GND	Ground	1B	Note1
39		GND	Ground	1A	Note1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	Note1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	Note1
46		Reserved	NC	3A	Note3
47		VS1	NC	3A	Note3
48		VccRx1	3.3V Power Supply	2A	Note2
49		VS2	NC	3A	Note3
50		VS3	NC	3A	Note3
51		GND	Ground	1A	Note1
52	CML-O	Rx7n	Transmitter Inverted Data Output	3A	
53	CML-O	Rx7p	Transmitter Non-Inverted Data Output	3A	
54		GND	Ground	1A	Note1
55	CML-O	Rx5n	Transmitter Inverted Data Output	3A	
56	CML-O	Rx5p	Transmitter Non-Inverted Data Output	3A	
57		GND	Ground	1A	Note1
58		GND	Ground	1A	Note1
59	CML-O	Rx6n	Transmitter Inverted Data Output	3A	
60	CML-O	Rx6p	Transmitter Non-Inverted Data Output	3A	

61		GND	Ground	1A	Note1
62	CML-O	Rx8n	Transmitter Inverted Data Output	3A	
63	CML-O	Rx8p	Transmitter Non-Inverted Data Output	3A	
64		GND	Ground	1A	Note1
65		NC	NC	3A	Note3
66		Reserved	NC	3A	Note3
67		VccTx1	3.3V Power Supply	2A	Note2
68		Vcc2	3.3V Power Supply	2A	Note2
69		Reserved	NC	3A	Note3
70		GND	Ground	1A	Note1
71	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
72	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
73		GND	Ground	1A	Note1
74	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
75	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
76		GND	Ground	1A	Note1

Notes:

[1] QSFP-DD uses common ground (GND) for all signals and supply (power) . All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

[3] All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B,B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Block Diagram of Transceiver

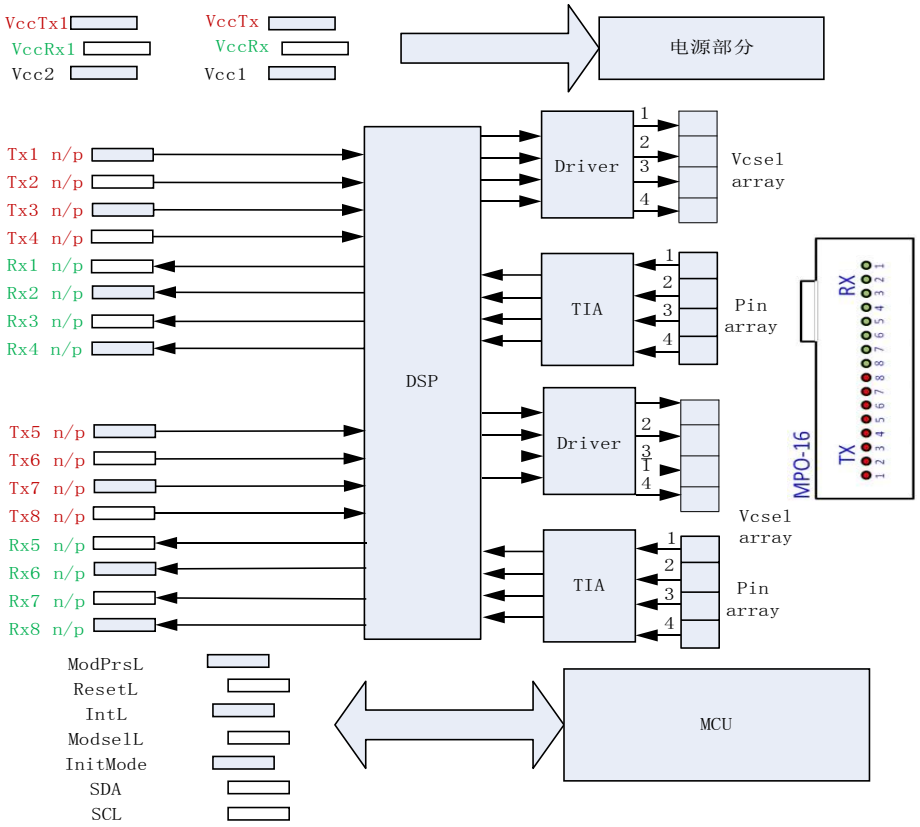

Figure2

Digital Diagnostic Memory Map

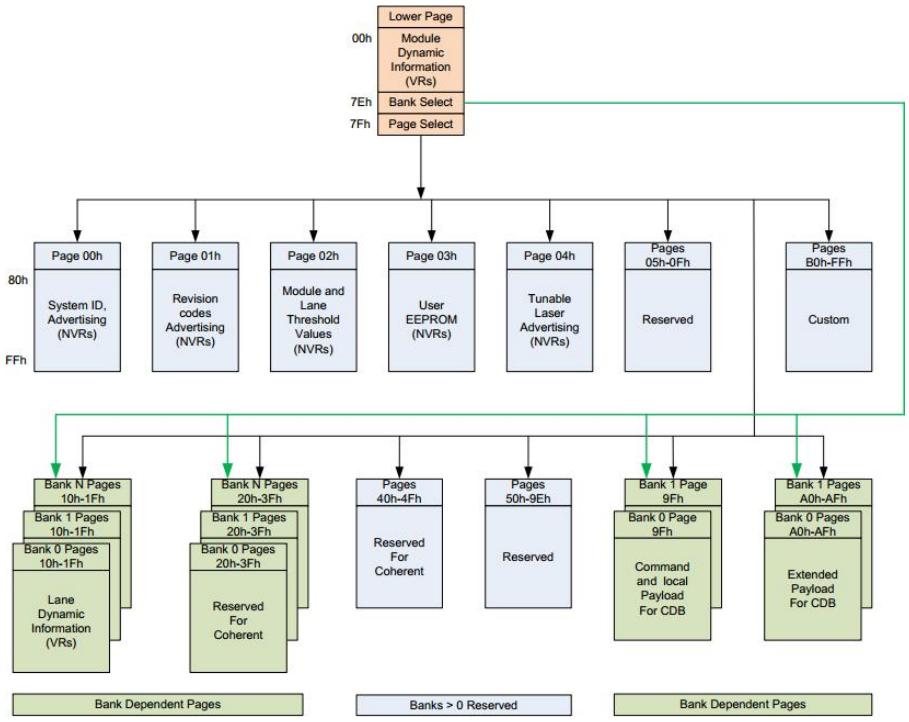

Figure4

EEPROM Information

CMIS rev4.0 defines a memory mapping in EEPROM, which describes the transceiver function, standard interface, manufacturer and other information. The information can be accessed through a 2-wire serial interface with an 8-bit address of 1010000x (a0h). The contents of the memory are shown in Table 8.

Table8-EEPROM Serial ID Memory Contents (A0h)

Page	Addr	Field Size Bytes	Name of Field	Hex	Description
	0	1	Identifier	0x18	QSFP-DD module, refer to SFF-8024
	1	1	Version ID	0x40	CMIS revision V4.0
	2	1	flate_men/CLEI/TWI max speed	0x00	Paged memory, Module supports up to 400 kHz
	3	1	Module state	*	Ready status
	4	1	Bank 0 lane 8-1 flag summary	*	No flag bits from bank 0
	5	1	Bank 1 lane 8-1 flag summary	*	No flag bits from bank 1
	6	1	Bank 2 lane 8-1 flag summary	*	No flag bits from bank 2
	7	1	Bank 3 lane 8-1 flag summary	*	No flag bits from bank 3
	8	1	Data Path firmware fault, Module firmware fault, L-Module state	ms	Note1

			changed flag		
	9	1	L-Vcc3.3V/Temp Low/High Warning/Alarm	ms	Latched warning flag, Relevant to the actual situation of the module
	10	1	L-Aux 2/1 Low/High Warning/Alarm	ms	Latched warning flag, Relevant to the actual situation of the module
	11	1	L-Vendor Defined/Aux 3 Low/High Warning/Alarm	ms	Latched warning flag, Relevant to the actual situation of the module
	12	1	Reserved	0x00	
	13	1	Custom	0x00	
	14	1	Module Monitor 1: Temperature MSB	ms	Internally measured temperature
	15	1	Module Monitor 1: Temperature LSB	ms	Internally measured temperature
	16	1	Module Monitor 2: Supply 3.3-volt MSB	ms	Internally measured 3.3V input supply voltage
	17	1	Module Monitor 2: Supply 3.3-volt LSB	ms	Internally measured 3.3V input supply voltage
	18	1	Module Monitor 3: Aux 1 MSB	0x00	Reserved
	19	1	Module Monitor 3: Aux 1 LSB	0x00	Reserved
	20	1	Module Monitor 4: Aux 2 MSB	0x00	Reserved
	21	1	Module Monitor 4: Aux 2 LSB	0x00	Reserved
	22	1	Module Monitor 5: Aux 3 MSB	0x00	Reserved
	23	1	Module Monitor 5: Aux 3 LSB	0x00	Reserved
	24	1	Module Monitor 6: Custom MSB	0x00	Reserved
	25	1	Module Monitor 6: Custom LSB	0x00	Reserved
	26	1	ForceLowPwr / Squelch control/ ForceLowPwr / Software Reset	0x60	Tx Squelch reduces Pave/No ForceLowPwr / Not in reset
	27-28	2	Reserved	0x00	
	29-30	2	Custom	0x00	
	31	1	Mask bit for Module State Changed Flag	0x00	No Mask bit for Module State Changed flag
	32	1	Mask bit for temp & supply 3.3V Low/high alarm/warning flag	0x00	No Mask bit for Vcc3.3/Temp Low/High Warning/Alarm
	33	1	Mask bit for AUX1 & AUX2 low/high alarm/warning flag	0x00	No Mask bit for Aux 2 / 1 Low / High Warning/Alarm
	34	1	Mask bit for AUX3&Vendor define low/high alarm/warning flag	0x00	No Mask bit for AUX3&Vendor define low/high alarm/warning flag
	35	1	Reserved flag mask	0x00	No Reserved flag mask
	36	1	Custom	0x00	
	37-38	2	CDB Status Area	0x00	
	39-40	2	Module Firmware Version	0x00	

	41-63	23	Reserved	0x00	
	64-82	19	Custom	0x00	
	83-84	2	Inactive Firmware Version	0x00	
	85	1	Module Type code	0x01	MMF
	86	1	ApSelCode 1: Host Electrical Interface Code	0x11	400G GAUI-8 C2M
	87	1	ApSelCode 1: Module Media Interface Code	0x10	400G BASE SR8
	88	1	ApSelCode 1: Host/Media LaneCount	0x88	8 Host lanes, 8 Media lanes
	89	1	ApSelCode 1: Host Lane Assignment	0x01	Permissible first host lane number for Application: lane 1
	90	1	ApSelCode 2: Host Electrical Interface ID	0xFF	End of the application list
	91	1	ApSelCode 2: Module Media Interface ID	0x00	No application for code 2
	92	1	ApSelCode 2: Host/Media LaneCount	0x00	No application for code 2
	93	1	ApSelCode 2: Host Lane Assignment	0x00	No application for code 2
	94-117	24	ApSelCode 3~ApSelCode 8	0x00	No application for code 3~8
	118-125	8	Password Entry and Change	0x00	The password entry function is used to control write access to the custom page 03h (EEPROM) and other custom upper pages.
	126	1	Bank Select Byte	0x00	Bank0 is accessed
	127	1	Page Select Byte	0x00	Upper page 00h is accessed
00h	128	1	Identifier	0x18	QSFP-DD module, refer to SFF-8024
00h	129	1	Vendor Name	0x48	“H”
00h	130	1	Vendor Name	0x47	“G”
00h	131	1	Vendor Name	0x20	“ ”
00h	132	1	Vendor Name	0x47	“G”
00h	133	1	Vendor Name	0x45	“E”
00h	134	1	Vendor Name	0x4E	“N”
00h	135	1	Vendor Name	0x55	“U”
00h	136	1	Vendor Name	0x49	“I”
00h	137	1	Vendor Name	0x4E	“N”
00h	138	1	Vendor Name	0x45	“E”
00h	139	1	Vendor Name	0x20	“ ”
00h	140	1	Vendor Name	0x20	“ ”
00h	141	1	Vendor Name	0x20	“ ”

00h	142	1	Vendor Name	0x20	“ ”
00h	143	1	Vendor Name	0x20	“ ”
00h	144	1	Vendor Name	0x20	“ ”
00h	145	1	Vendor OUI	0xDA	
00h	146	1	Vendor OUI	0x28	
00h	147	1	Vendor OUI	0xEC	
00h	148	1	Vendor PN	0x4D	“M”
00h	149	1	Vendor PN	0x51	“Q”
00h	150	1	Vendor PN	0x44	“D”
00h	151	1	Vendor PN	0x2D	“-”
00h	152	1	Vendor PN	0x31	“1”
00h	153	1	Vendor PN	0x32	“2”
00h	154	1	Vendor PN	0x46	“F”
00h	155	1	Vendor PN	0x31	“1”
00h	156	1	Vendor PN	0x43	“C”
00h	157	1	Vendor PN	0x20	“ ”
00h	158	1	Vendor PN	0x20	“ ”
00h	159	1	Vendor PN	0x20	“ ”
00h	160-163	4	Vendor PN	0x20	“ ”
00h	164	1	Vendor rev	0x31	V1.0
00h	165	1	Vendor rev	0x30	V1.0
00h	166-181	16	Vendor SN	ms	
00h	182-187	6	Date Code	ms	
00h	188	1	Lot Code	0x00	
00h	189	1	Lot Code	0x00	
00h	190-199	10	CLEI code	0x20	
00h	200	1	Module Card Power Class	0XA0	Power Class 6
00h	201	1	Max Power	0x2C	11W
00h	202	1	Cable Assembly Length: Length multiplier field/base Length field	0x00	
00h	203	1	Media Connector Type	0x28	MPO 1×16
00h	204	1	Copper Cable 5 GHz attenuation	0x00	Passive copper cable attenuation at 5 GHz in 1 dB increments
00h	205	1	Copper Cable 7 GHz attenuation	0x00	Passive copper cable attenuation at 5 GHz in 1 dB increments
00h	206	1	Copper Cable 12.9 GHz attenuation	0x00	Passive copper cable attenuation at 12.9 GHz in 1 dB increments
00h	207	1	Copper Cable 25.8 GHz attenuation	0x00	Passive copper cable attenuation at 25.8 GHz in 1 dB increments
00h	208-209	2	Reserved	0x00	
00h	210	1	Near end implementation	0x00	Lane1-8 implemented in near end

00h	211	1	Implemented lanes in far end	0x00	Undefined - Use for detachable modules
00h	212	1	Media Interface Technology	0x00	850 nm VCSEL
00h	213-220	8	Reserved	0x00	
00h	221	1	Custom	0x00	
00h	222	1	Checksum	cc	Note2
00h	223-255	29	User Custom Info	0x00	non-volatile storage space for information provided by the original manufacturer of the module.
01h	128	1	Module firmware major revision	0x01	V1.0
01h	129	1	Module firmware minor revision	0x00	V1.0
01h	130	1	Module hardware major revision	0x01	V1.0
01h	131	1	Module hardware minor revision	0x00	V1.0
01h	132	1	Base Length (SMF)	0x00	Link length multiplier for SMF fiber 00 = 0.1 (1 to 6.3 km) 01 = 1 (1 to 63 km) 10, 11 = reserved
01h	133	1	Length (OM5)	0x32	Transmission distance:100m
01h	134	1	Length (OM4)	0x32	Transmission distance:100m
01h	135	1	Length (OM3 50um)	0x23	Transmission distance:70m
01h	136	1	Length (OM2 50um)	0x00	
01h	137	1	Reserved	0x00	
01h	138	1	Wavelength (high order byte)	0x42	Central wavelength:850nm
01h	139	1	Wavelength (low order byte)	0x68	Central wavelength:850nm
01h	140	1	Wavelength tolerance (high order byte)	0x07	Wavelength tolerance:10nm
01h	141	1	Wavelength tolerance (low order byte)	0XD0	Wavelength tolerance:10nm
01h	142	1	Diagnostic pages /Page 03 /Banks implemented	0x04	User page 03h/ Bank0 implemented
01h	143	1	ModSelL wait time exponent /mantissa	0XF0	2.048ms
01h	144	1	DataPathDeinit_MaxDuration or ModulePwrDn_MaxDuration,DataPathInit_MaxDuration	0x47	50 ms <= DataPathDeinit < 100 ms 1 s <= maximum state duration < 5 s
01h	145	1	Cooling implemented/Tx input clock recovery capabilities/Aux Monitor	0x00	module requires all Tx input lanes to be in a single Tx synchronous group.
01h	146	1	Maximum module temperature	0x46	70℃
01h	147	1	Minimum module temperature	0x00	0℃
01h	148	1	Propagation Delay MSB	0x00	Not specified
01h	149	1	Propagation Delay LSB	0x00	Not specified

01h	150	1	Minimum operating voltage	0x9D	3.14V
01h	151	1	Detector type,RX Output Eq type,Rx Optical Power Measurement type,Rx LOS type,Rx LOS fast mode implemented, Tx Disable fast mode implemented, Module-Wide Tx Disable	0x18	PIN detector. Peak-to-peak amplitude stays constant, or not implemented, or no information. Rx Optical Power Measurement type=average power. Rx LOS responds to Pave. Rx LOS fast mode/Tx Disable fast mode not implemented. Tx Disable implemented per lane.
01h	152	1	Per lane CDR Power	0x00	
01h	153	1	Rx Output Amplitude code 0011b/ 0010b/ 0001b/ 0000b implemented	0xFA	Rx Output Amplitude code 0010b /0001b/0000b/0011b implemented. Tx Input Equalization control for manual / fixed programming : 10dB
01h	154	1	Max Rx Output Eq Post / Pre-cursor	0x77	Max supported value of the Rx Output Eq Post/Pre-cursor 7/3.5dB
01h	155	1	Wavelength control, Tunable transmitter, Tx Squelch / Force Squelch / Squelch Disable / Disable / Polarity Flip implemented	0x2B	No wavelength control, Transmitter not tunable, Tx Squelch Disable not implemented, Tx Squelch / Force Squelch /Tx Disable/ Polarity Flip implemented
01h	156	1	Rx Squelch / Disable / Polarity Flip implemented	0x03	Rx Squelch not implemented. Disable/ Polarity Flip implemented
01h	157	1	Tx Adaptive Input Eq Fault/CDR LOL/LOS/Fault flag implemented	0x06	Tx CDR/LOS flag implemented, Tx Fault not implemented
01h	158	1	Rx LOL/LOS flag implemented	0x06	Rx LOL/LOS flag implemented
01h	159	1	Custom , Aux 3/2/1, Internal 3.3 Volts, Temperature monitor implemented	0x03	Internal 3.3 Volts/Temperature monitor implemented.
01h	160	1	Tx Bias current measurement and threshold multiplier,Rx Optical Input Power/Tx Output Optical Power/Tx Bias monitor implemented	0x07	Rx Optical Input Power / Tx Output Optical Power / Tx Bias monitor implemented.
01h	161	1	Tx Input Eq Store/Recall buffer count,Tx Input Eq Freeze,Adaptive Tx Input Eq, Tx Input Eq fixed manual control, Tx CDR Bypress control, Tx CDR implemented	0x09	CDR cannot bypass
01h	162	1	Staged Set 1, Rx Output Eq control, Rx Output Amplitude control, Rx CDR Byprass	0x1D	CDR cannot bypass

			control, Rx CDR implememted		
01h	163-175	13	Reserved	0x00	
01h	176	1	Media Lane Assignment Options, ApSel 0001b	0x01	Permissible first Media lane number for ApSel 0001b: lane 1
01h	177-190	14	Media Lane Assignment Options, ApSel 0001b-1111b	0x00	No application for code 2-15
01h	191-222	32	Custom	0x00	
01h	223-250	28	ApSelCode 9-15: Host Electrical Interface Code / Module Media Interface Code	0x00	No application for code 9-15
01h	251-254	4	Reserved	0x00	
01h	255	1	Checksum	cc	The checksum code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 130 to byte 254
02h	128	1	Temperature monitor high alarm threshold MSB	0x50	80℃
02h	129	1	Temperature monitor high alarm threshold LSB	0x00	80℃
02h	130	1	Temperature monitor low alarm threshold MSB	0xF6	-10℃
02h	131	1	Temperature monitor low alarm threshold LSB	0x00	-10℃
02h	132	1	Temperature monitor high warning threshold MSB	0x46	70℃
02h	133	1	Temperature monitor high warning threshold LSB	0x00	70℃
02h	134	1	Temperature monitor low warning threshold MSB	0x00	0℃
02h	135	1	Temperature monitor low warning threshold LSB	0x00	0℃
02h	136	1	Supply 3.3-volt monitor high alarm threshold MSB	0x8D	3.63V
02h	137	1	Supply 3.3-volt monitor high alarm threshold LSB	0xCC	3.63V
02h	138	1	Supply 3.3-volt monitor low alarm threshold MSB	0x74	2.97V
02h	139	1	Supply 3.3-volt monitor low alarm threshold LSB	0x04	2.97V
02h	140	1	Supply 3.3-volt monitor high warning threshold MSB	0x87	3.465V
02h	141	1	Supply 3.3-volt monitor high	0x5A	3.465V

			warning threshold LSB		
02h	142	1	Supply 3.3-volt monitor low warning threshold MSB	0x7A	3.135V
02h	143	1	Supply 3.3-volt monitor low warning threshold LSB	0x76	3.135V
02h	144-151	8	Aux 1 monitor high/low alarm, high /low warning	0x00	Reserved
02h	152-159	8	Aux 2 monitor high/low alarm, high /low warning	0x00	
02h	160	1	Aux 3 monitor high alarm threshold MSB	0x00	
02h	161	1	Aux 3 monitor high alarm threshold LSB	0x00	
02h	162	1	Aux 3 monitor low alarm threshold MSB	0x00	
02h	163	1	Aux 3 monitor low alarm threshold LSB	0x00	
02h	164	1	Aux 3 monitor high warning threshold MSB	0x00	
02h	165	1	Aux 3 monitor high warning threshold LSB	0x00	
02h	166	1	Aux 3 monitor low warning threshold MSB	0x00	
02h	167	1	Aux 3 monitor low warning threshold LSB	0x00	
02h	168-175	8	Custom monitor high/low alarm, high /low warning	0x00	Reserved
02h	176	1	Tx optical power monitor high alarm threshold MSB	0x9B	6dBm
02h	177	1	Tx optical power monitor high alarm threshold LSB	0x83	
02h	178	1	Tx optical power monitor low alarm threshold MSB	0x05	-8.5dBm
02h	179	1	Tx optical power monitor low alarm threshold LSB	0X85	
02h	180	1	Tx optical power monitor high warning threshold MSB	0x62	4dBm
02h	181	1	Tx optical power monitor high warning threshold LSB	0X1F	
02h	182	1	Tx optical power monitor low warning threshold MSB	0x08	-6.5dBm
02h	183	1	Tx optical power monitor low warning threshold LSB	0xBF	
02h	184	1	Tx bias current monitor high	0x13	10mA

			alarm threshold MSB		
02h	185	1	Tx bias current monitor high alarm threshold LSB	0x88	
02h	186	1	Tx bias current monitor low alarm threshold MSB	0x00	0mA
02h	187	1	Tx bias current monitor low alarm threshold LSB	0x00	
02h	188	1	Tx bias current monitor high warning threshold MSB	0x11	9mA
02h	189	1	Tx bias current monitor high warning threshold LSB	0x94	
02h	190	1	Tx bias current monitor low warning threshold MSB	0x00	0mA
02h	191	1	Tx bias current monitor low warning threshold LSB	0x00	
02h	192	1	Rx optical power monitor high alarm threshold MSB	0x9B	6dBm
02h	193	1	Rx optical power monitor high alarm threshold LSB	0x83	
02h	194	1	Rx optical power monitor low alarm threshold MSB	0x03	-10.4dBm
02h	195	1	Rx optical power monitor low alarm threshold LSB	0x90	
02h	196	1	Rx optical power monitor high warning threshold MSB	0x62	
02h	197	1	Rx optical power monitor high warning threshold LSB	0X1F	4dBm
02h	198	1	Rx optical power monitor low warning threshold MSB	0x05	
02h	199	1	Rx optical power monitor low warning threshold LSB	0XA5	-8.4dBm
02h	200-229	30	Reserved	0x00	
02h	230-254	25	Customizable space	0x00	
02h	255		Checksum	cc	The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 254.

Note:

[1] ms: Manufacturer-selected value, which may be relevant to the actual situation of the module.

[2] cc: Checksum code. Checksum is a one-byte code that can be used to verify that the read-only static data is vaild

Ordering Information

Table9-ordering information

Part No	Specification								
	Package Type	Rate	Tx	Pout	Rx	Sen (OMA)	T_{op}	Reach	Other
OTQDD-40X85-SR8	QSFP-DD	400G	850nm VCSEL	-6.5 ~ 4dBm	PIN	max (-6.5, SECQ-7.9)	0~70 ℃	70m(OM3) 100m(OM4)	DDM/ RoHs